

Dr. R.Pavithra Guru, M.E., Ph.D.

Assistant Professor

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Dr R. Pavithra Guru is currently employed as an Assistant Professor within the Department of Computer Science and Engineering at SRMIST in Ramapuram, Chennai. The individual has nearly six years of experience conducting research and delivering instruction. In addition to their formal qualifications, they have also obtained certifications in various courses offered by NPTEL. The individual in question obtained a Doctor of Philosophy degree in VLSI Physical Design from Sri Sivasubramaniya Nadar College of Engineering, affiliated with Anna University Chennai, in 2022. The individual in question has disseminated his research findings through the publication of articles in national and international scholarly journals and through presentations at conferences and symposiums. The individual possesses a comprehensive understanding of the theoretical underpinnings of the subject matter, as well as the practical considerations involved in designing applications within this field. The individual possesses a high level of knowledge and proficiency in Very Large Scale Integration (VLSI) Design, focusing on Physical Design, Micro Electronics, and algorithms. Additionally, the individual possesses a strong understanding of correlated disciplines such as Wireless Sensor Networks and Robotics.

Area of Research:

VLSI Design, CAD Algorithms, Wireless Sensor Networks and Robotics

Selected Publications:

- Published a paper entitled as. “An efficient VLSI circuit partitioning algorithm based on satin bower bird optimisation (SBO)”. Journal of Computational Electronics – Springer 19, 1232–1248 (2020).
- Published a paper entitled as "Website Vulnerability Scanner".. Journal of Population Therapeutics and Clinical Pharmacology, 30(15), 43–53 2023).
- R. Pavithra Guru, V.Vaithianathan “Enhanced Partitioning of VLSI Circuits based on Grey Wolf Optimization (GWO) algorithm” - Expert Systems With Applications – (Revision Submitted - Elsevier).
- R. Pavithra Guru, V.Vaithianathan “A study on GCA based partitioning approach for VLSI Physical Design” - Applied Soft Computing– (Under Review - Elsevier).
- Published a paper entitled as “OTG Module for High Speed Transmission” in International Journal of Scientific, Engineering and Technology (IJSET) on April 2016. ISSN:2277-1581 Volume No.5 IssueNo.4, pp: 180-183.

List of Conference Papers

- Presented a paper entitled as "Ant Colony Optimization Based Partition Model for VLSI Physical Design," 2020 International Conference on Computer Communication and Informatics (ICCCI),Coimbatore, India, 2020.
- Presented a paper titled as “On The Go implementation of FPGA“ in 2rd International Conference on Technical Innovations in Electrical, Electronics and Computer and Communications” (ICTIEECC) held at PET Engineering College,Vallioor on 23 March 2016.
- Presented a paper entitled as “Verilog Module for On The Go Implementation” in“IEEE sponsored International Conference on Energy Efficient Technologies for Sustainability” (ICEETS) held at St.Xavier’s Catholic College of Engineering,Nagercoil on 7 April – 8 April, 2016.
- Presented a paper entitled as “CNN Based Food Calorie Recognition For Dietary Assessment in“IETE sponsored International Conference on Power of Artificial Intelligence and Machine Learning for Human Empowerment held at Sri Venkateswara College of Engineering, Pennalur, Sriperumbudur. On 20 May – 21 May, 2022.
- Presented a paper entitled, "Cloud Computing Based Workload Optimization using Long Short Term Memory Algorithm," 2022 Third International Conference on Smart Technologies in Computing, Electrical and Electronics (ICSTCEE), Bengaluru, India, pp. 1-7, on April 18,2022.

List of Patents

- Dr.R.Pavithra Guru. "Method for Designing A Very Large Scale Integration (VLSI) Circuit." Indian Patent Application 202241035401 A, filed June 24, 2022.
- Dr.V.Samuthira Pandi, Dr.S.Nagarajan, Dr.M.Ayyadurai, Dr. Judy Simon, Dr.R.Pavithra Guru, Dr. Amirthalakshmi .TM “4G and 5G Technology Based Several- Antennas for Smartphone App using Multimode” Indian Patent Application 202241042837 A, filed July 29, 2022.
- Ms. G.indumathi, Dr. R.Pavithra Guru, Ms. K.Srilekha, Mr. Ezravethamani “AI BASED SMART WALKING STICK FOR VISUALLY IMPAIRED WITH ALERTING UNIT” Indian Patent Application 81345, Patent Number 369641-001 A, filed December 23, 2022.

Reviewer of Journals

- 1.Journal of Intelligent & Fuzzy Systems, IOS Press, Netherlands
- 2.Journal of Supercomputing, Springer, USA
- 3.Scanning , Hindawi

Membership of Scientific / Engineering Bodies

- 1.Member, Indian Society for Technical Education (ISTE)
- 2.Member, Institution of Engineers (India)
- 3.Member, Institute of Electrical and Electronics Engineers (IEEE)